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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,181	12/02/2003	Richard Thomas Plunkett	PEA01US	6713

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER	
KAU, STEVEN Y	

ART UNIT	PAPER NUMBER
2625	

MAIL DATE	DELIVERY MODE
06/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,181	PLUNKETT ET AL.	
	Examiner	Art Unit	
	STEVEN KAU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Continued Examination Under 37 CFR 1.114: A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 25, 2008 has been entered.

Response to Arguments

2. This action is responsive to the following communication: an Amendment filed on March 25, 2008.

- Applicant's arguments with respect to Claims 1-5 have been fully considered but are moot in view of the new ground(s) of rejection due to the amendments. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The examiner also references the applicant to the claims rejection section below for the explanation on how the prior art references read on the amended claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2 & 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al (Yamashita) (US 5,701,505) in view of Shimizu et al (Shimizu) (US 5,031,034).

Regarding claim 1.

Yamashita discloses a method **(e.g. halftone processing method of col 20, line 30)** for sequentially outputting full lines of dither values **(e.g. threshold data)** of a dither matrix stored in a memory **(e.g. dither matrices are contained in the halftone circuits, col 20, line 43 through col 21, line 11)**, comprising the step of: (a) reading a plurality of dither values of the dither matrix from the memory **(col 20, line 43 through col 21, line 11)**, commencing at an initial start position in the memory until a full line of dither values of the dither matrix has been read **(e.g. Yamashita discloses a 6-block parallel processing, the one-line data is processed during the one cycle of the sync signal, thus initial staring position for each line of data must be adjusted for fetching the right data, col 20, lines 5-6 and col 20, line 63 through col 21, line 11)**; (c) updating the initial start position to an updated start position in the memory of a subsequent line of dither values **(e.g. Yamashita discloses a parallel processing**

apparatus which processing data in block cycles, thus the starting position in the memory must be updated in each period to support the data and halftoning process, Fig. 27, col 18, lines 35-45 & col 20, line 63 through col 21, line 11); (d) reading a plurality of dither values from the memory, commencing at the updated start position until the full subsequent line of dither values has been read (**e.g. Yamashita discloses a halftone process, which includes four halftone-process circuits where a row of dither values or threshold data are read from memory for the respective image data in a parallel processing in bloc cycles as discussed above, thus, each updated starting position of a row of a line of dither value or threshold data must be commenced; Fig. 27, col 18, lines 35-45 & col 20, line 63 through col 21, line 11**); and (f) repeating steps (c)-(e) until all lines of dither values of the dither matrix have been read (**e.g. steps c-e must be repeated because Yamashita employs a parallel processing apparatus which processing data in block cycles; Figs. 38 & 39, col 23, lines 17-23**).

Yamashita does not explicitly teach (b) outputting the full line of dither values read in step (a) to a buffer memory; and (e) outputting the full line of dither values read in step (d) to a buffer memory.

Shimizu teaches (b) outputting the full line of dither values read in step (a) to a buffer memory (**e.g. line buffers store the output of threshold circuit, Fig. 7 & col 5, lines 18-26**); and (e) outputting the full line of dither values read in step (d) to a buffer memory (**Fig. 7, col 5, lines 18-26**).

Having a method of Yamashita' 505 reference and then given the well-established teaching of Shimizu' 034 reference, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the halftone process method of Yamashita' 505 reference to include (b) outputting the full line of dither values read in step (a) to a buffer memory; and (e) outputting the full line of dither values read in step (d) to a buffer memory as taught by Shimizu' 034 reference since doing so would increase the processing speed for color halftone process and further the line buffers provided could easily be implemented for one another with predictable results.

Regarding claim 2.

Yamashita discloses wherein a plurality of dither matrices are stored in the memory (**e.g. dither matrices are contained in the halftone circuits, which implies that dither matrices are stored in the memory of the circuitry, col 20, line 43 through col 21, line 11**), and wherein steps (a), (d) and (f) include reading a plurality of dither values from at least two of the dither matrices simultaneously (**e.g. Yamashita discloses a parallel processing apparatus which processing data in block cycles, i.e. Fig. 27 teaches a process of outputting 4 lines; in order to support the parallel processing, the halftone-processing circuits 751-754 must reading at least two of the dither matrices simultaneously as shown in Figs 32-25 & col 20, line 63 through col 21, line 11**).

Regarding claim 4.

Yamashita discloses wherein, in repeated step (c), it is determined whether dither values at an end position in the memory have been read, and if so, the updated start position is updated to the initial start position **(e.g. Yamashita discloses a parallel processing apparatus, which processing data in block cycles, thus the starting position in the memory must be updated by determining if dither value or threshold data is at the end of the matrix position in each period to support the data and halftoning process, Fig. 27, col 18, lines 35-45 & col 20, line 63 through col 21, line 11)**.

Regarding claim 5.

Yamashita discloses wherein, in repeated step (c), it is determined whether dither values at an end position in the memory have been read for each of the dither matrices, and if so, the updated start position is updated to the initial start position **(e.g. Yamashita discloses a parallel processing apparatus, which processing data in block cycles, thus the starting position in the memory must be updated by determining if dither value or threshold data is at the end of the matrices position in each period to support the data and halftoning process, Figs. 27 & 32-25, col 18, lines 35-45 & col 20, line 63 through col 21, line 11)**

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al (Yamashita) (US 5,701,505) in view of Shimizu et al (Shimizu) (US 5,031,034) as applied to claim 1, and further in view of Matsuba et al (Matsuba) (US 5,815,286).

Regarding claim 3.

Yamashita does not explicitly teach wherein the dither matrices are of different sizes.

Matsuba discloses wherein the dither matrices are of different sizes (**Figs. 1a-c & col 7, lines 9-18**).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Yamashita combined with Shimizu to include that dither matrices are of different sizes taught by Matsuba and therefore, four color components can be processed with respect to four threshold matrices value at the same time (Figs 21A-D, col 20, lines 21-32).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Kau whose telephone number is 571-270-1120 and fax number is 571-270-2120. The examiner can normally be reached on M-F, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Poon can be reached on 571-272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Steven Kau/
Examiner, Art Unit 2625
6/3/2008

/King Y. Poon/
Supervisory Patent Examiner, Art Unit 2625